National Aeronautics and Space Administration

FY25 Strategic University Research Partnership (SURP)

High-efficiency high-power GaN amplifiers chips for next-generation planetary radar and space communications

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OBJECTIVES

This project advances solid-state transmitter technology to meet the demanding requirements of deep space communications and planetary radar. By enhancing both efficiency and output power at the MMIC level with advanced fabrication processes, it directly supports the next generation of scalable, reliable space transmitters. The immediate objective is to achieve record efficiency and output power in solid-state RF electronics at X-band (8.5 GHz) and Ka-band (32 GHz)—the core frequencies for NASA's Deep Space Network (DSN) and ground-based radar systems. These improvements enable a phased-array roadmap in which individual nodes deliver 10–80 kW, scaling to megawatt-class power for high-resolution planetary radar imaging and deep space target detection. At the spacecraft level, the work supports compact, low-power X- and Ka-band transmitters, reducing reliance on bulky power-combining stages. The result is a transformative capability for planetary defense, radar science, and sustained deep space communications.

BACKGROUND

Recent advances in wide-bandgap (WBG) semiconductors, particularly GaN on SiC, enable high-power microwave electronics with strong potential for deep space communication and ground-based planetary radar. Achieving both high output power and high efficiency is essential but difficult, involving trade-offs between performance and manufacturability. Solid-state approaches using circuit and spatial power-combining techniques are especially attractive: unlike klystrons or traveling-wave tubes, which fail abruptly, semiconductor devices degrade gracefully at comparable power levels. The Planetary Science Decadal Survey (NASEM 2022, Planetary Defense Section) and a KISS report (Lazio 2021) identify this technology as a priority. Ultra-high power could reduce the complexity of spatial combining architectures, while high power-added efficiency (PAE) lowers waste heat. Yet, the commercial semiconductor market offers little incentive to meet NASA's niche requirements—extreme power, efficiency, bandwidth, and thermal margins—making sustainable access to custom MMIC foundries challenging. To address this, JPL and university partners have collaborated with foundries to design and test advanced MMICs, simultaneously validating fabrication models. A proposed partnership would expand this model, embedding student projects tailored to NASA/JPL constraints, while advancing next-generation semiconductor solutions for planetary defense and space communication.

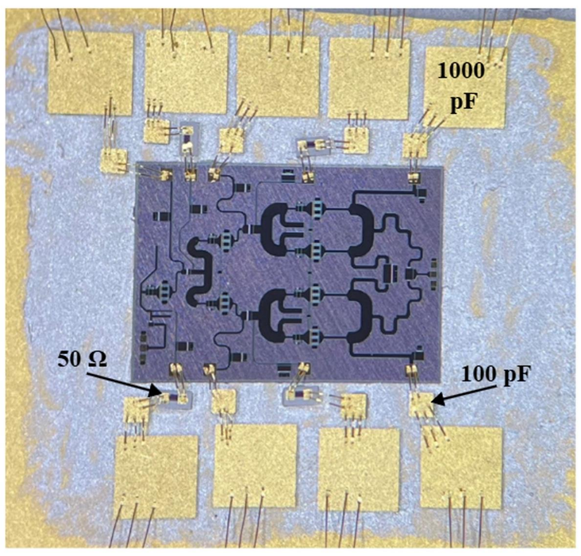

Fig.1. Photograph of fabricated PA mounted on a CuMo carrier and bonded to off-chip 100 pF and 1000 pF capacitors for dc-biasing. Each gate pad is also bonded to a 50 Ω series resistor to help with stability. The chip in the center of the photograph is 5 mm × 3 mm.

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SIGNIFICANCE OF RESULTS/BENEFITS TO NASA/JPL

The work directly supports NASA STMD Explore: Communications and Navigation 2022 priorities—"High-Efficiency Solid-State Power Amplifiers," "Harsh Environment Communications," and "Low-cost, reliable, high-power DSN transmitters to 1 MW at up to 34 GHz." It also aligns with the 2020 KISS planetary radar study (Lazio 2021) and the Planetary Defense section of the recent decadal survey (NASEM 2022). Beyond strategic value to JPL, this effort strengthens the DSN, Goldstone Solar System Radar, and next-generation phased-array planetary radar systems. High-efficiency, solid-state transmitters are also critical to the Artemis program, supporting sustained lunar exploration by enabling robust communications between lunar surface assets, Gateway, and Earth. Reliable, compact, and power-efficient transmitters will be essential for Artemis landers, rovers, and small spacecraft, all constrained by size, weight, and power budgets. The partnership further benefits broader mission classes—deep space constellations, planetary landers, and rovers—by offering low-voltage, miniaturized mid-to-high power (>10 W) solid-state alternatives to traveling-wave tubes. Seed funding will empower the JPL–university team to pursue opportunities such as STMD's CIF for low-TRL MMIC designs, University-led TechFlights, and the Small Spacecraft Program, advancing next-generation communications for planetary defense, exploration, and Artemis.

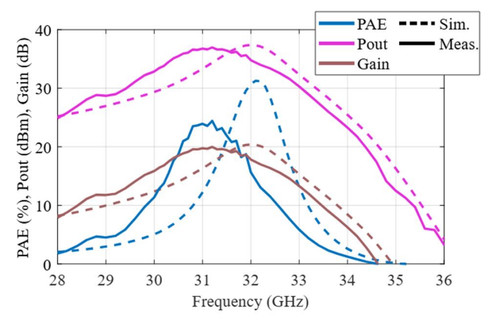

Fig.2. Measured vs. simulated large-signal performance at 17 dBm input power at VDS =28V. The total quiescent current for all devices is 420 mA, and all stages are biased at the same current as in the simulations.

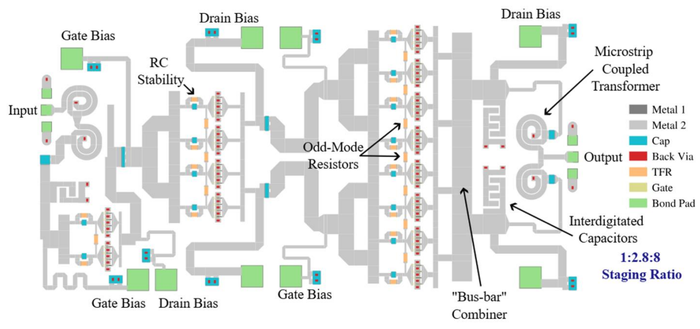

Fig.3. Final layout of the 3-stage power combined PA designed using the Qorvo 150 nm GaN on SiC process. The device peripheries used in each stage are as follows: two 8×25 μm devices in the first stage; four 8×35 μm devices in the second stage; and eight 8×50 μm devices in the final stage. The total design dimensions are 5 mm × 2.5 mm.

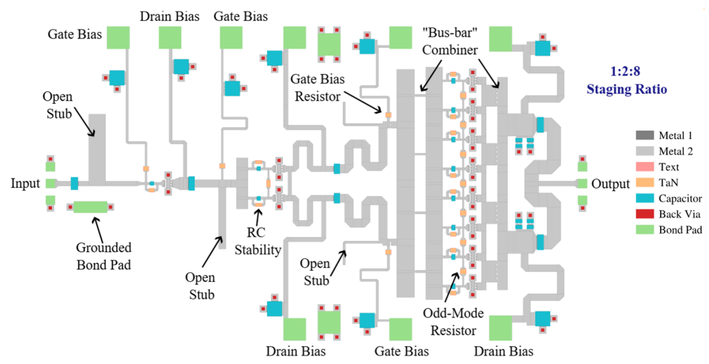

Fig.4. Final layout of the 3-stage power combined PA designed using the HRL 40 nm GaN on SiC. The devices used peripheries of each stage are as follows: one 6×37.5 μm devices in the first stage; two 6×37.5 μm devices in the second stage; and eight 6×37.5 μm devices in the final stage. The total design dimensions are 5 mm × 3 mm

ACKNOWLEDGMENTS

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APPROACH AND RESULTS

The Ka-band power amplifier designed using the WIN NP12 process from Spring of 2024 (Fig. 1) is measured over frequency and input power. Measured results show 5 W output power with 20 dB of gain and 24% power-added-efficiency (PAE) at 31.2 GHz (Fig. 2). Four additional power amplifiers have been designed and taped out since last year's report using three total GaN-on-SiC technologies (WIN NP12 120nm; Qorvo QGaN15 150nm; HRL T3L 40 nm) and are currently under fabrication. Each of these technologies is chosen for high output power (3W or greater per chip) and efficiency (30% - 40%) at Ka-band. The first PA is a redesign of the measured one, now taking into account newly updated device models and thermal effects to minimize discrepancies between measurement and simulation. The redesign achieves (2.5 dB) higher peak gain than the original, 5 W output power and 30% efficiency at 80°C device temperature. Secondly, a 3-stage PA using the Qorvo QGaN15 is designed using a bus-bar combiner at the output. This combining technique is largely unexplored for high-power GaN PAs at millimeter-wave frequencies and is well-suited for efficient, chip-level combining of many devices to achieve high output powers. Eight individual devices are combined at the output stage, efficiently utilizing vertical space allocated for the chip. This design has a simulated output power of 10W with 25 dB of saturated gain and 28% PAE at 32 GHz. The final chip sent for tape out includes two of these PAs side-by-side, potentially allowing for close to 20 W output power, per chip, using off-chip combining. Finally, the HRL T3L process is used to design a 2-stage and 3-stage PA. Notably, this technology has a significantly smaller gate length of 40nm compared to both previously discussed technologies, resulting in lower overall power handling per device, but significantly higher PAE. For these reasons, the designs using this process are focused primarily on achieving high efficiency (near 40%). Both the 2 and 3-stage versions share the same output stage topology, using an eight-element bus-bar combiner to reach 3 W of output power. The 2-stage iteration has a simulated saturated gain of 17 dB while the 3-stage version, shown in Fig. reaches 28 dB of saturated gain. Both PA designs using the HRL process demonstrate up to 45% simulated PAE when driven into saturation.

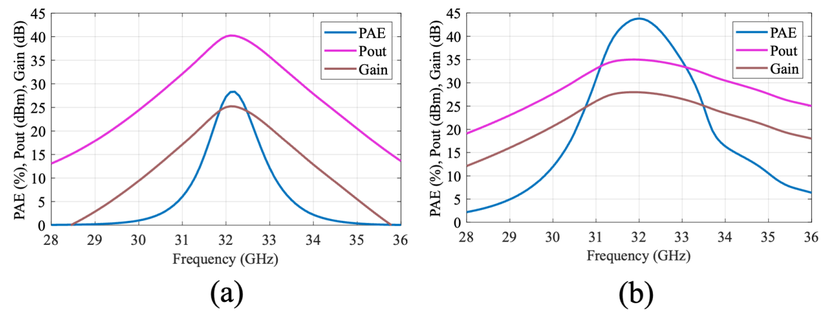

Fig.5. (a) Simulated large signal performance of the PA designed using the Qorvo QGaN15, showing 40 dBm of output power, 28% PAE, and 25 dB of saturated gain at 32 GHz. (b) Simulated large signal performance of the PA designed using HRL T3L, showing 35 dBm of output power, 44% PAE, and 28 dB of saturated gain at 32 GHz.

PUBLICATIONS

[1] J. Molles, S. Rahimizadeh, L. Yi and Z. Popović, "Multi-Watt GaN MMIC Power Amplifiers for 32 GHz Deep Space Communications and Radio Science," 2025 United States National Committee of URSI National Radio Science Meeting (USNC-URSI NRSM), Boulder, CO, USA, 2025
[2] Jack Molles and Zoya Popović, "5-Watt Ka-Band Power Amplifiers in a 120-nm GaN MMIC Process," submitted to 2026 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR), Los Angeles, CA, 2026.

REFERENCES

[1] [Lazio 2021] Lazio, Joseph, et al. "Next-Generation Ground-Based Planetary Radar." (2021).
[2] [NASEM 2022] National Academies of Sciences, Engineering, and Medicine. "Origins, Worlds, and Life: A Decadal Strategy for Planetary Science and Astrobiology 2023-2032." (2022).

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