National Aeronautics and Space Administration

FY24 Strategic University Research Partnership (SURP)

High-efficiency high-power GaN amplifiers chips for next-generation planetary radar and space communications

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OBJECTIVES

The overall technical goal is to significantly enhance the power efficiency and output power at the customized monolithic microwave integrated circuits (MMICs) level with advanced fabrication processes, enabling next-generation future solid-state transmitters for space applications. The specific objective of this student project is to have solid-state RF electronics reaching an unprecedented efficiency at X-band (8.5GHz) or Ka-band (32GHz) with an unprecedented high output power, and provide a scalable power-combining road map towards phased-array-based planetary radar with 10-80kW at each node, reaching MegaWatt combined power into deep space. The project is also expected to influence the design of solid-state spacecraft transmitters at X and Ka -bands with no or fewer power-combining layers at a lower needed output power.

BACKGROUND

Semiconductor-based microwave electronics have advanced significantly in the past decade. Wide-bandgap semiconductor materials such as Gallium-Nitride on SiC hold the promise to achieve very high power at microwave frequencies. Achieving high power and high efficiency simultaneously is important for next-generation ground-based solar system radar as well as space communication. By utilizing circuit and spatial microwave power combining techniques, the solid-state semiconductor solution is attractive due to its graceful-degradation feature at a comparable power level to the traditional klystron and traveling tube technologies, which typically stop working without any pre-failure symptoms. This direction has been prioritized in the recent planetary decadal survey [NASEM 2022] (Planetary Defense Section) as well as a KISS report in 2020 [Lazio 2021]. Ultra-high output power may greatly reduce the layers and units of the spatial power combining units. An ultra-high power-added-efficiency (PAE) will greatly reduce the wasted heat that must be dissipated. Achieving high efficiency and power output simultaneously is challenging and requires many tradeoffs when the commercial market force has to be considered. NASA's ground-based planetary radar and deep space communication pose a unique niche requirement on both efficiency and power. However, this is a negligible market for the semiconductor industry for JPL to sustainably access highly customized MMICs foundry with a reasonable cost. For a long time, the foundries have been collaborating with our university partner group to design and fabricate highly customized MMICs to test, verify and improve their most advanced fabrication models and processes. The proposed partnership aims to formulate student projects to meet NASA/JPL's special constraints on the MMICs, e.g. power, efficiency, bandwidth, supplying voltage, margin, etc.

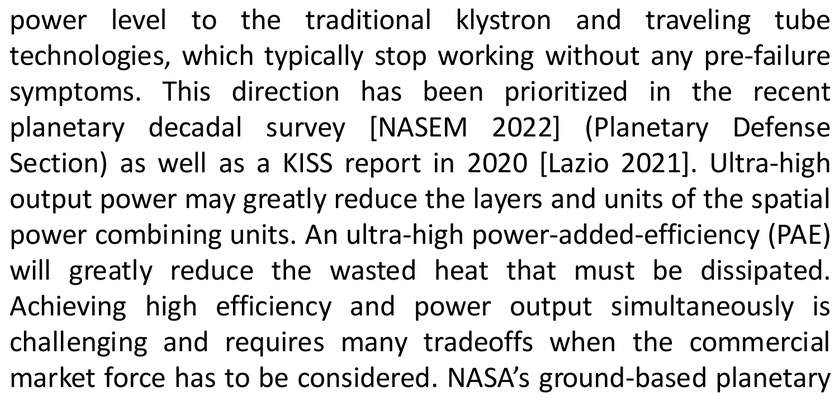

Fig.1. Layout of the WIN chip that is currently in fabrication (expected delivery in October 2024). The chip is 5 mm by 3 mm in size.

SIGNIFICANCE OF RESULTS/BENEFITS TO NASA/JPL

The proposed work directly addresses NASA STMD Explore: Communications and Navigation 2022 – Top Priorities - "High-Efficiency Solid-State Power Amplifiers", "Harsh Environment Communications", "Low-cost, reliable, high power-DSN transmitters based on tubes or solid-state to 1Megawatt at up to 34GHz", as well as next-generation planetary radar of 2020 KISS Study [Lazio 2021] and the Planetary defense section stated in the recent planetary decadal survey[NASEM 2022]. In addition to the strategic value to JPL, the partnership has the potential to benefit DSN and most planetary missions that rely on DSN, Goldstone solar system radar and next-generation phase-array-based planetary radar. It also benefits future space missions that can benefit from carrying low-voltage, miniaturized mid-high power (>10Watt) solid-state transmitters as an alternative to the commonly used travel-wave tubes. Examples include deep space single or constellation of small spacecraft missions, small landers and rovers missions on planetary surfaces which have stringent size, weight, and power constraints while the communication transmitters constitute a significant portion in most cases. The proposed partnership and seed funding will empower the JPL-University team to write strong proposals to programs such as STMD's CIF for low TRLs MMICs designs, University-led TechFlights and Small Spacecraft program.

Fig.2. *Simulated performance versus frequency of the PA currently under fabrication in the WIN Semiconductors NP12 process, showing a peak power of over 6W with a saturated gain over 23dB and a power-added efficiency of 34%.*

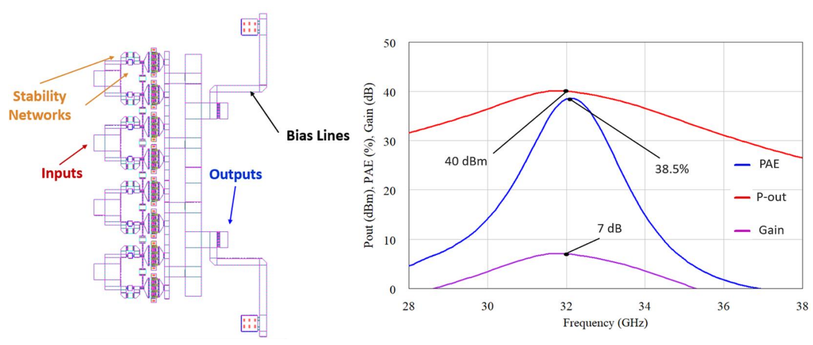

Fig.3. *Left: Layout of the output power-combined stage with eight 8x3um devices. Right: Simulated performance versus frequency of the PA currently under design in the Qorvo QGaN15 process showing a peak output power of 40dBm with a final-stage gain of 7dB and a PAE of close to 40%.*

ACKNOWLEDGMENTS

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REFERENCES

[1] [Lazio 2021] Lazio, Joseph, et al. "Next-Generation Ground-Based Planetary Radar." (2021).
[2] [NASEM 2022] National Academies of Sciences, Engineering, and Medicine. "Origins, Worlds, and Life: A Decadal Strategy for Planetary Science and Astrobiology 2023-2032." (2022).

APPROACH AND RESULTS

The goal of the project is to use advanced GaN semiconductor processes to achieve as high output power from a single chip as possible at 32GHz for space communications. Another equally important goal is to maximize the power-added efficiency, which requires high gain from the GaN process. To achieve over 5 to 10W of output power from a GaN MMIC power amplifier at 32GHz, several foundries available through partnerships to the group at CU Boulder have been considered: (1) WIN Semiconductors NP12 120-nm GaN on 2-mil SiC; (2) BAE Systems 140-nm GaN on 2-mil SiC; and (3) Qorvo QGaN15 150nm GaN on 2-mil SiC process. These processes are available in the following order: (a) WIN NP12 tapeout out in May 2024; (b) QGaN15 design is due for tapeout at the end of September 2024; and (c) BAE 140nm does not yet have a tapeout date.

The PA designed in WIN NP12 had a space of 5mm x 3mm available, allowing for a 3-stage amplifier with a 1:2:4 staging ratio. The final stage HEMTs are 6x100um device, and there are 4 devices combined using reactive corporate combiners. This process has a specified power density of 3.75W/mm at 28V drain bias, which gives an ideal maximum of 9W output power. However, power density is lower when efficiency is a target, and there are losses in the combiners and matching networks, so we expect about 6W of output power from these 4 devices. The two branch drivers are 6x100um devices, providing sufficient power to saturate the output stage. The pre-driver HEMT is also a 6x100um device, since other device sizes did not show better power or efficiency. The simulated performance versus frequency of the PA currently under fabrication in the WIN Semiconductors NP12 process shows a peak power of over 6W with a saturated gain over 23dB and a power-added efficiency of 34% at 32GHz. The simulations are performed with a foundry nonlinear model and using Cadence AWR MWO harmonic balance simulator.

The PA currently under design in the QGaN15 process, which has a larger node (150nm) than the WIN process (120nm), but higher power density (>4W/mm). To reach close to 10W of output power, several on-chip power combining approaches are considered, and we are proceeding with a design that combines eight 8x35um devices in a "power bar" configuration with a 4:1 reactive combiner at the output. The output stage reaches peak output power of 40dBm with a final-stage gain of 7dB and a PAE of close to 40%. The relatively low available gain at 32GHz impacts the PAE. The driving stages are currently under design for a 2:4:8 staging ratio, and the entire chip is predicted to measure about 5mm by 3mm.

The potential for the BAE Systems 140-nm process is investigated initially with load-pull using the nonlinear models extracted at BAE for wideband applications, and as a function of device size. The resulting peak power and efficiency from a 8x75um device show over 2W output power with PAE=40%.

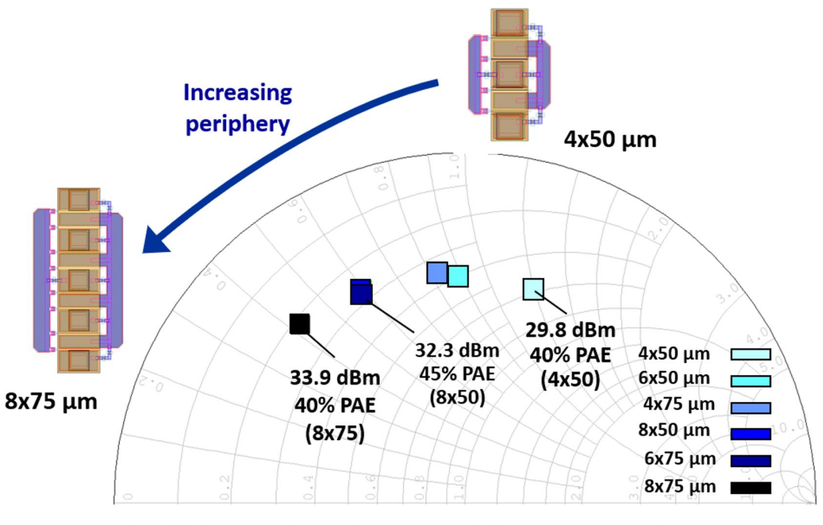

Fig.4. *Load-pull data performed on several device sizes in the BAE Systems 140-nm GaN-on-SiC process. The plot shows that as the periphery of the device increases, the power also increases, while the power-added efficiency sees a 5 percentage point decrease. This is the first part of a design that helps determine the staging ratio.*

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