National Aeronautics and Space Administration

FY24 Topic Areas Research and Technology Development (TRTD)

Low-power giga sampling digitizer for large-format far-IR detectors

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Strategic Focus Area: Components and Integrated Systems

Objective:

- Develop a low-power giga-sampling digitizer for JPL's far-IR detector systems
  - ➢ Read up to 2,000 pixels of microwave kinetic inductance detectors (MKIDs)
  - ➢ Application-specific integrated circuit (ASIC) using 65 nm CMOS process
  - ➢ Time-interleaved (TI) architecture to achieve 2 GS/s sampling rate
  - ➢ ≤ 100 mW power consumption

Background:

- PRIMA (The PRobe far-Infrared Mission for Astrophysics) mission
  - MKIDs with over 10,000 pixels for high-sensitivity far-IR and sub-mm astronomy
  - ➢ *Challenge:*
    - ✓ Current solutions lack low-power, compact MKID readout electronics
  - ➢ *Solution*:
    - ✓ Development of a power-efficient, single-chip digitizer ASIC
    - ✓ Integration with spectrometer ASICs, optimized for large-format MKID arrays.

Approach and Results:

- *Architecture*
  - ➢ 32-way TI-SAR ADC
    - ✓ TI successive approximation register (TI-SAR) A2D converter
    - ✓ Each sub-channel operates at a minimum 62.5 MS/s speed
    - ✓ Achieving 2+ GS/s with the fully-integrated digitizer architecture
  - ➢ Two additional reference channels for linearity and timing mismatch calibration
  - ➢ Off-chip digital calibration engine

- *SAR ADC design*
  - ➢ 11-bit non-binary split capacitive D2A converter (CDAC)
    - ✓ CDAC split into upper 6-bit (C12-C6) and lower 5-bit (C5-C0) arrays
    - ✓ Reducing input load capacitance (~470 fF)
  - ➢ Asynchronous clocking scheme with a self-timed clock generator
    - ✓ To avoid distributing high-speed clocks.
    - ✓ internal clock generator triggered by a comparator.

- *Simulation results*
  - ➢ Performance improvement after linearity calibration
  - ➢ Sub-channel ADC consumes ~0.85 mW at 62.5 MS/s with a 1 V supply.
  - ➢ Total power consumption for 34 ADCs and peripherals is ~50 mW.
    - ✓ Well below the 100 mW target

Significance and Benefits to NASA and JPL :

- Miniaturized MKID readout electronics for next-generation far-IR detectors.
  - ➢ Significant reduction in power consumption
    - ✓ 10x improvement over traditional off-the-shelf methods.
  - ➢ single-chip MKID solution in the PRIMA far-IR observatory, planned for the 2030s

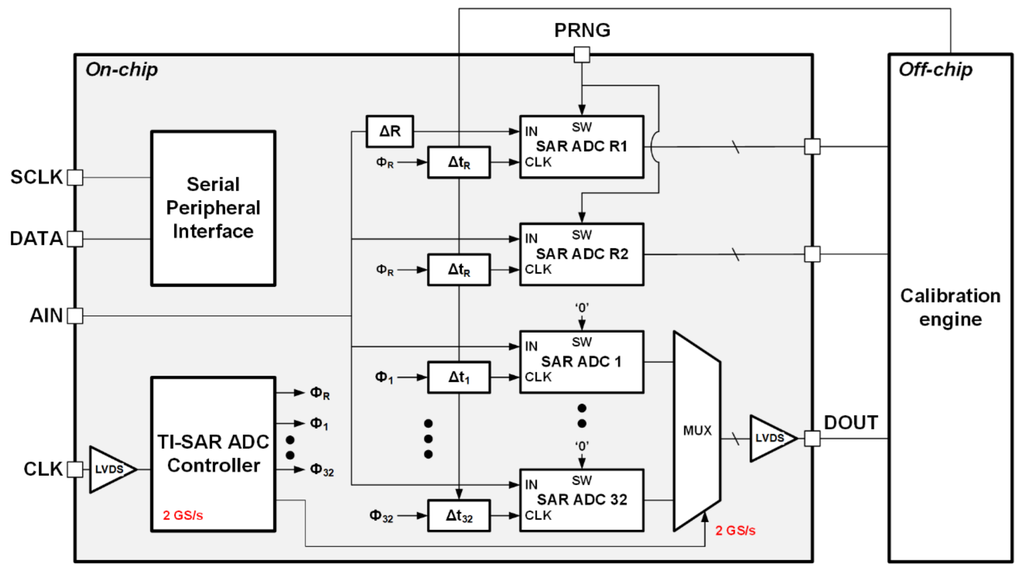

Figure 1 The digitizer architecture

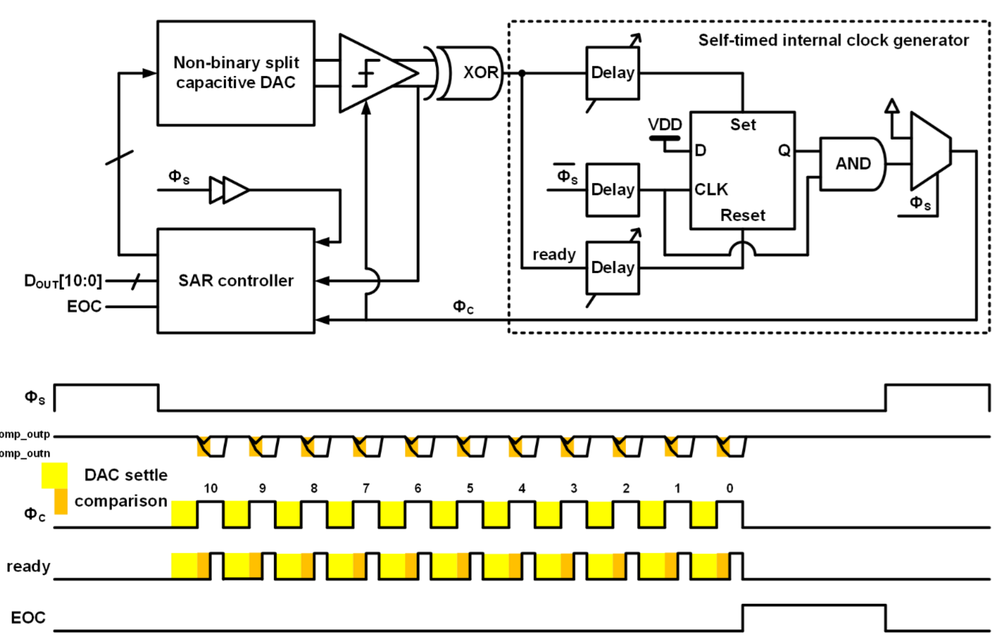

Figure 2 Sub-channel SAR ADC architecture and timing diagram

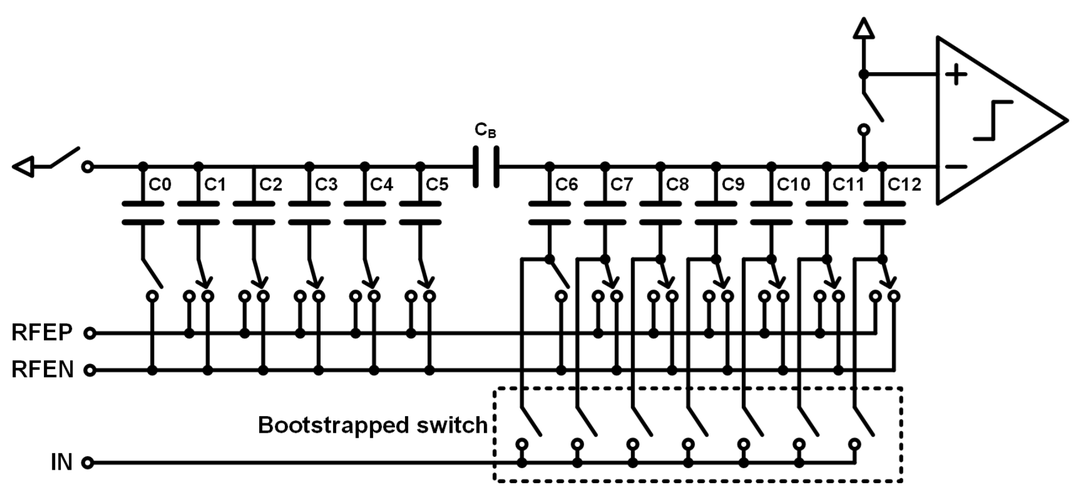

Figure 3 The 11-b non-binary split capacitive DAC

	One sub-channel ADC	Fully integrated digitizer
Architecture	SAR	32× TI-SAR
Number of ADCs	1	34 (with two references)
Sampling rate	≥ 62.5 MS/s	≥ 2 GS/s
Resolution	11 bits (1b redundancy)	
SNDR	≥ 50 dB	
Power	≤ 1mW	≤ 50 mW (goal: 100 mW)
Area	~ 0.04 mm^2	~ 2 mm^2 (except for on-chip decoupling capacitors)

Table 1 Performance summary of one-subchannel (simulated) and fully integrated digitizer (estimated)

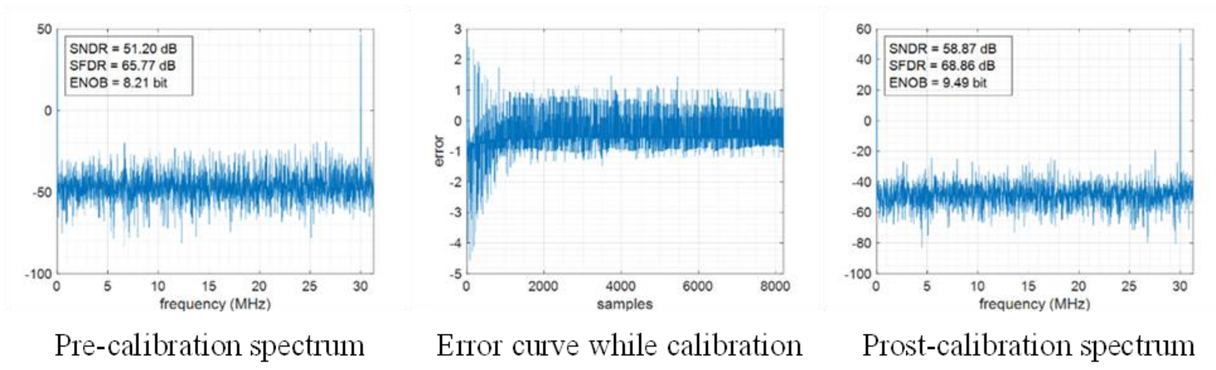

Figure 4 Simulated results of sub-channel SAR ADC

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Publications:

Taehoon Kim, "Modeling and Simulation of Microwave Kinetic Inductance Detectors Readout System using Simulink and RF Blockset," submitted to *IEEE Transactions on Applied Superconductivity.*

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