National Aeronautics and Space Administration

FY24 Topic Areas Research and Technology Development (TRTD)

Direct Energy Transfer Solar Array Architecture with Inherent Array Collapse Prevention

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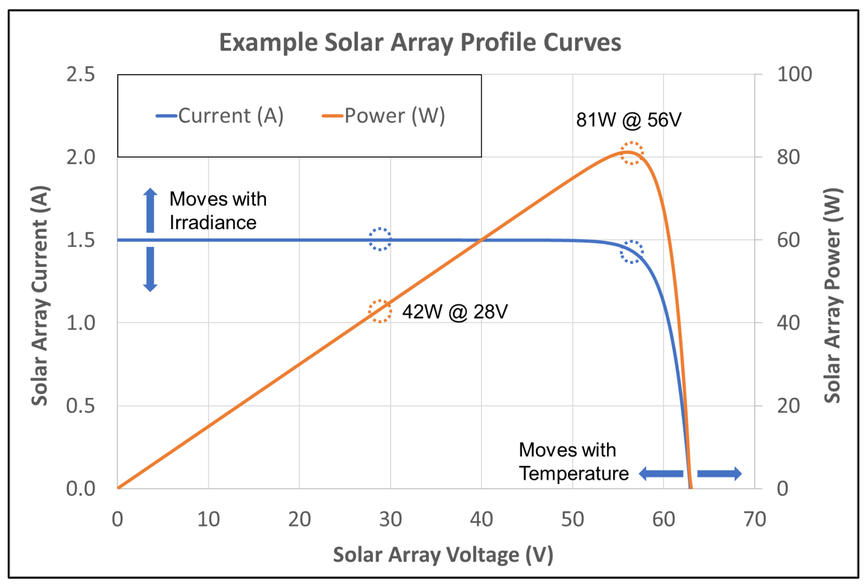
Support: Troy Gross (349F)

Strategic Focus Area: Power generation

BACKGROUND

Energy sources like Solar Arrays and Radio-isotope Thermoelectric Generators, have a characteristic Current – Voltage profile where there is nominally a single maximum power point



Energy transfer to a battery is maximized by operating at this point. By slowly adjusting the duty cycle (**D**) of a power converter, the voltage of the source is adjusted without compromising the stability of the system.

Buck Converter Transfer Function

$$V_{out} = D \cdot V_{in}$$

$$V_{in} = \frac{V_{out}}{D}$$

Solar Array Voltage

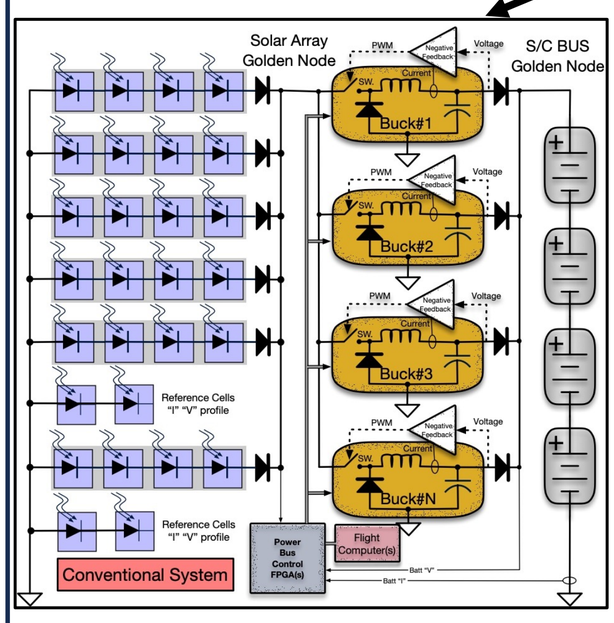
Stiff Battery Voltage

Control Input

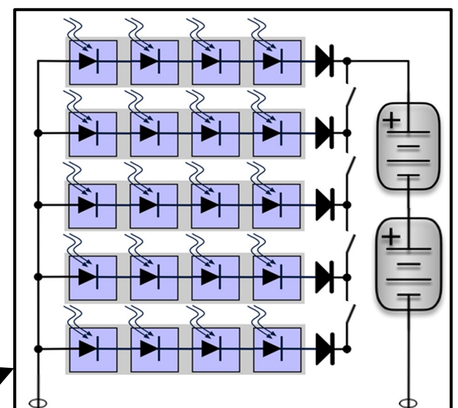
Controlled 'Output'

CONVENTIONAL SYSTEMS

State of the Art



Uses DC/DC converters with negative feedback, and can require large capacitive banks to mitigate stability concerns



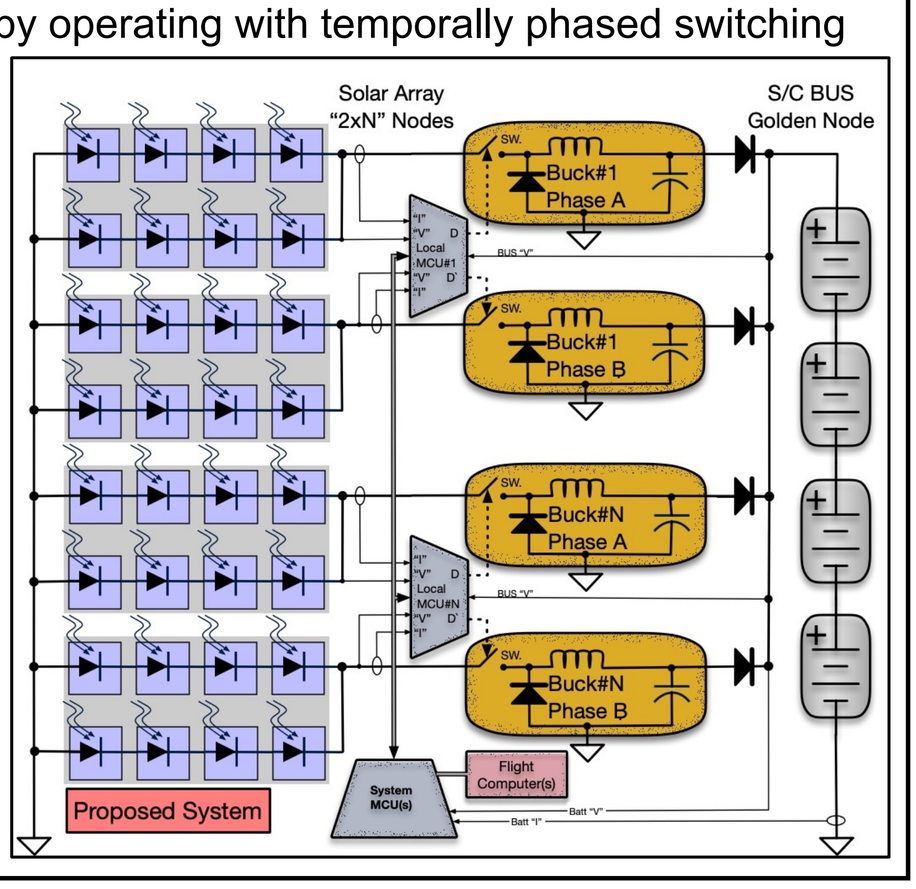
String Switchers

String switchers are simple and Robust. They operate by directly connecting the Solar Array to the Battery. The battery voltage is lower than the solar array maximum power voltage, resulting in less power transferred to the battery.

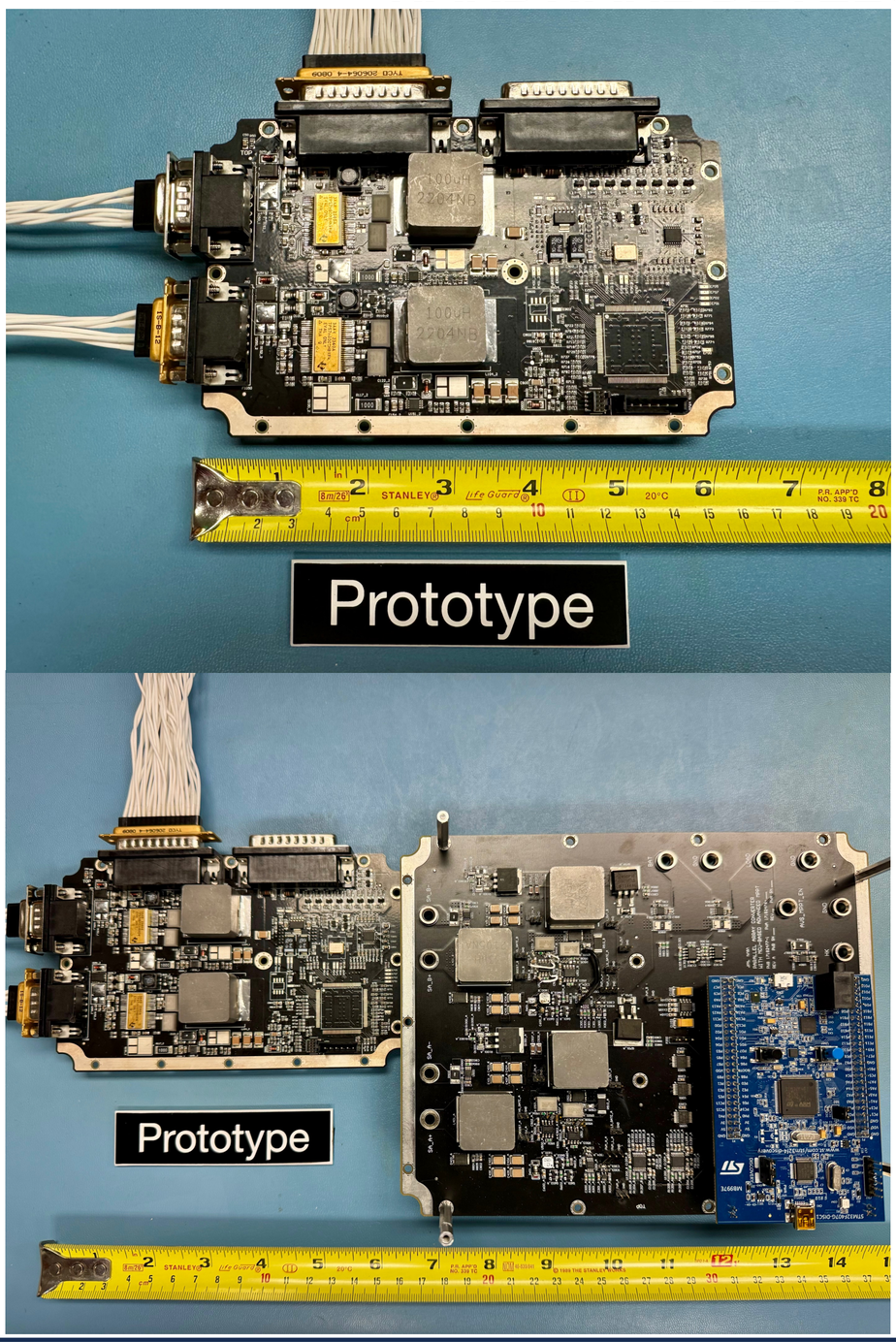
PROPOSED SYSTEM

Key Technology Features

- Ensures stability by transferring energy from a source to a storage element via an effectively open loop switching regulator
- Converges to and operates at the Maximum Power Point of the energy source by using a simple perturb & observe algorithm running on a Rad-Hard MCU
- Generates I-V profiles of the energy source without dedicated test cells
- Optimizes noise characteristics by operating with temporally phased switching
- Optimizes conversion efficiency by utilizing GaN switches and smart diode circuits



HARDWARE DEVELOPMENT



FY24 Hardware Prototype

- Rad-Hard Vorago MCU and Power stages reside on a single PWB
- FY24 PWB is 160mm long by 100mm wide with 160cm^2 surface area
- FY24 PWB layout conforms to new 3U form factor for distributed power
- Fully populated FY24 PWB weighs 300g

FY24 Hardware Prototype vs. FY23

- 2023 PWB was 200mm long by 160mm wide with 320cm^ 2 surface area
- FY24 PWB is 20% shorter, 37.5% narrower with 50% less surface area.

MCU DEVELOPMENT

A Time-Triggered Embedded System, written in C, showed 97-99% convergence to the MPP

ARM CORTEX M4 MicroController
Breadboard: STMicro STM32F407
Path to Flight: Vorago VA41630 [200krad]

Main Clock [100MHz]	GPIO Discrete Inputs & Outputs	Operational State Machine	Timers [Sync & PWM]	PWM [Phase A]
				PWM [Phase B]
Task Scheduler [SysTick Timer]	Data & Event Logger	DET / P&O	Interface	UART
		Fractional Voc		JTAG
		Current Limiting		SPI
		Recovery		[TBC]

ADC								
Panel 1 Voltage	Panel 1 Current	Panel 2 Voltage	Panel 2 Current	Battery Voltage	Buck 1 Voltage	Buck 2 Voltage	Output Current	Load Current

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